Cost-Effective High-Performance Monolithic *X*-Band Low-Noise Amplifiers

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Abstract—**A low-cost, high-performance *X*-band amplifier with ion-implanted MESFET technology has been demonstrated. Various design, material, and processing approaches have been evaluated in terms of yield, cost, and device performance. An average noise figure of 2.2 dB and a standard deviation of 0.1 dB, with an associated gain of 22.5 dB and a standard deviation of 0.8 dB at the center frequency band of 9.5 GHz, have been measured.**

I. Introduction

RECENTLY, there has been a growing need for large quantities of inexpensive microwave and millimeter-wave monolithic components for active-array radar applications. The major issue facing the use of active-array antennas in radar system design is affordability. The affordability is further clouded by a lack of valid data from which performance and cost estimates can be made. In general, about 3000 to 10000 MMIC chips are needed to support a typical radar system. Therefore, a high-rate GaAs MMIC chip fabrication must be developed to increase throughput and reduce the chip cost.

In this paper, we will describe a cost-effective technology to fabricate high-performance GaAs *X*-band low-noise amplifiers (LNA). The discussion includes design considerations, material approach, and processing techniques which are essential to achieve our low-cost, high-performance objectives.

II. Circuit Design

The circuit design of the LNA has evolved as a result of both circuit refinements and new GaAs materials. To systematically improve the yield and performance, four design iterations have been carried out. A single FET geometry and the same basic circuit design were used for all four iterations. The first two versions were based on an existing FET fabricated by ion implantation into Cr-doped GaAs [1]. The first iteration LNA had 20 dB of gain and a 4-dB noise figure [2]. The second version flattened the gain response across the 9-to-10-GHz range, while keeping the same noise figure. In order to improve the noise figure, the third and fourth versions were based on FET's using VPE and ion implantation into liquid encapsulated Czochralski (LEC) substrates. These FET's had very similar characteristics, but were significantly different from the original FET fabricated on Cr-doped substrates. Between each iteration, we comprehensively evaluated not only the FET devices, but also the passive components in the monolithic circuits to determine the necessary layout modification. When the new *S*-parameters and equivalent noise model were incorporated, the final LNA design provided a circuit with a predicted 22 dB of gain and a 2.2-dB noise figure.

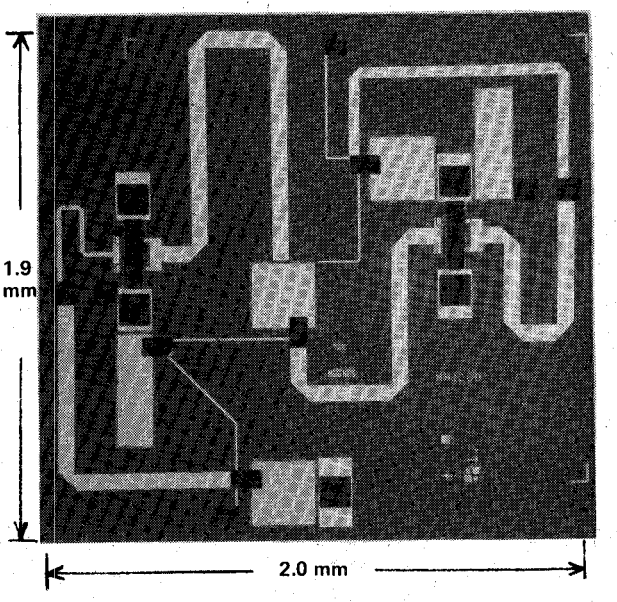

Fig. 1. *X*-band two-stage monolithic low-noise amplifier.

The final monolithic amplifier consists of two 0.5-μm-gate FET's with 300-μm gate width, five 10-pF overlay capacitors, microstrip lines, and via holes to ground. The chip size is 1.9 mm $\times$ 2.0 mm, as shown in Fig. 1.

III. Sensitivity Analysis

To ensure repeatable performance of the monolithic circuits, it is extremely important to design these circuits so that they are insensitive to material and process variations during the wafer processing. This can be achieved in the early circuit design stage by choosing appropriate circuit topology and optimum matching circuit elements. For this producibility study, we analyzed a number of key

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TABLE I
SENSITIVITY FACTOR FOR X-BAND LOW-NOISE AMPLIFIERS

$$\text{Sensitivity} = \frac{\text{FET parameter variation}}{\text{material/process parameter variation}}.$$

PARAMETER	GAIN		
	9 GHz	9.5 GHz	10 GHz
FET PARAMETERS			
Ri	-0.0062	-0.026	-0.046
Cgs	0.77	0.64	-1.06
Cgd	-0.32	-0.27	-0.23
Rd	1.09	0.92	0.87
gm	4.06	4.40	4.57
Substrate Thickness	0.73	1.04	0.92
Conductor Thickness	-0.012	-0.05	-0.043
Capacitor	0.14	0.16	0.14

TABLE II
EFFECTS OF MATERIAL AND PROCESS VARIATIONS ON THE FET EQUIVALENT CIRCUIT ELEMENTS

$$\text{Sensitivity} = \frac{\text{FET parameter variation}}{\text{material/process parameter variation}}.$$

Material/Process Parameters	Statistical Variation (%)	Sensitivity Factor				
		RI	CSG	GM	GD	CD
Doping Concentration	±10	-1.0	-1.0	+1.0	+1.0	-
Gate Length	± 5	-0.5	+1.0	-0.5	-0.5	-1.0
Channel Thickness	± 5	-1.0	-1.0	-1.0	+1.0	-

TABLE III
X-BAND LOW-NOISE AMPLIFIER—FABRICATION APPROACH

PROCESS	APPROACH
STARTING MATERIAL	LEC WAFER
ACTIVE LAYER	DIRECT ION IMPLANTATION
ISOLATION	MESA ETCH AND PROTON BOMBARDMENT
GATE	OPTICAL LITHOGRAPHY 1350B PROCESS Al AND Ti/Pt/Au 0.5 μm Lg 75 μm Zw
OVERLAY METAL	1.5 μm, Ti/Au, LIFTOFF
CAPACITOR	SPUTTERED SiO_2, 2000 Å
AIRBRIDGE	YES
VIA HOLE	YES
FINAL THICKNESS	4 MIL

parameters that had dominant effects on amplifier performance and derived their corresponding sensitivity factors. The sensitivity factor is defined as the unit performance variation divided by the unit circuit parameter variation. Table I summarizes the calculated sensitivity factors for the low-noise amplifier gain across the 9-to-10-GHz frequency band.

The analysis showed that the capacitance variation had a large effect on amplifier gain. Since we had established a very tight control on the capacitance value (~ 3 percent) in our overlay capacitor fabrication, it did not threaten the amplifier performance. In addition, variations in FET parameters (R_i, C_{gs}, G_{ds}, and g_m) should be related to the material and process variations more directly to reveal the significance of each parameter. Based on our present material and processing technology, we estimated the correlation between the material and processing variations and the FET circuit model elements (Table II). Using this table, we can concentrate on material and processing parameters which have a major effect on the performance, or we can change the circuit design to absorb variations more effectively.

IV. MMIC FABRICATION

A low-cost, high-yield process has been developed for the monolithic low-noise amplifier fabrication [3], [4]. Batch wafer processing (typically six wafers per lot) is used to simulate production conditions and minimize the labor costs. The MMIC fabrication procedure includes formation of the FET channel layer, device isolation, fabrication of ohmic contacts, Schottky gates, overlay metallization for circuitry, MOM overlay capacitors, device passivation, airbridge interconnects, wafer thinning, via hole etching, and back metallization. The process approach is summarized in Table III.

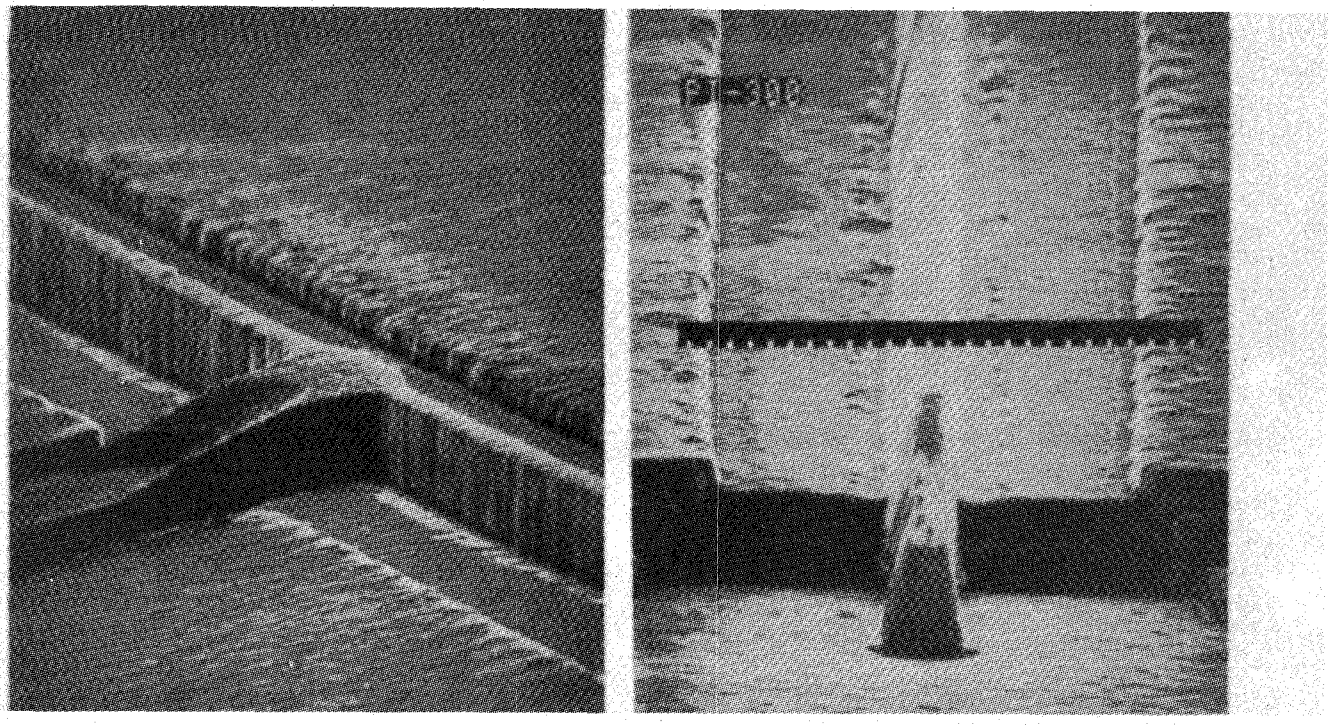

Fig. 2. Hughes 0.5-μm-gate low-noise FET fabricated by contact photolithography.

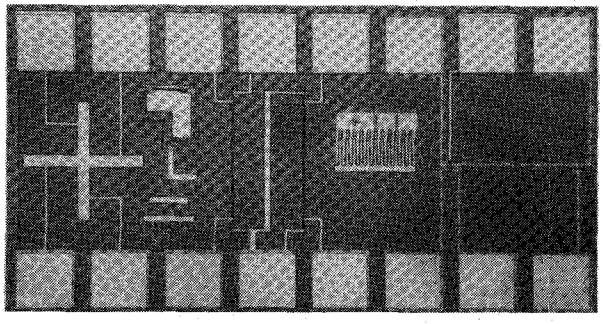

Fig. 3. NBS cross-bridge patterns for measuring gate length and alignment accuracy.

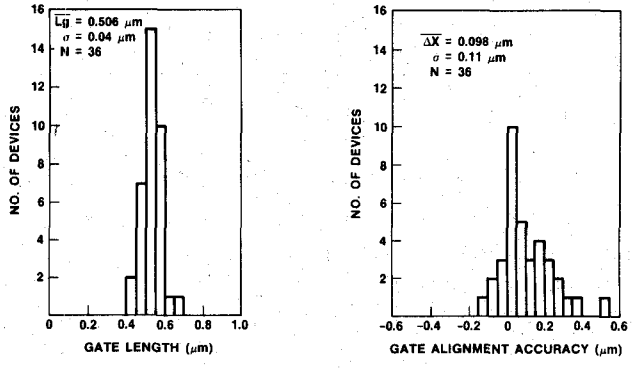

Fig. 4. Histogram of 0.5-μm gate length and alignment accuracy control.

The key to fabricating the low-cost, high-yield, high-performance, low-noise MMIC's is the use of ion implantation into qualified substrates. The FET channel layer is formed by directly implanting Si ions into an undoped LEC semi-insulating GaAs substrate at 7×10^{12} cm^{-2} dose and 100 keV energy. The implants are activated by capless annealing at 850°C to form an optimum low-noise FET channel layer. An important aspect of high-yield GaAs FET fabrication is the utilization of high-quality starting materials. Undoped LEC materials provide high quality and consistency; however, screening tests are still necessary to ensure good device yield and reproducibility. Substrate-related effects and problems are defined and monitored by using standard process-control monitoring techniques, such as $C-V$ profiles, I_{SAT} current, sheet resistivity, and FET characteristics measurements.

Device isolation is then achieved by a combination of mesa etching and proton implantation. Low-resistance source/drain ohmic contacts, essential for the low-noise FET performance, are formed by evaporating AuGe/Ni/Au and alloyed at 380°C in an N_2–H_2-forming gas atmosphere. This process yields a smooth surface suitable for subsequent gate definition, and a low contact resistance which is consistently below 0.25 Ω-mm.

The gate fabrication is the most critical process determining the device performance and yield. An optical contact lithography process is used to produce high-yield 0.5-μm gates (illustrated in Fig. 2) with higher throughput and more reliable equipment than a direct-write E-beam process. With the former process, a throughput of over ten wafers per hour with a yield of 80 percent or higher is achieved. Recess etch, metal deposition, and lift-off of gates are also crucial processes for good metal adhesion to the GaAs surface and low gate resistance for short gates. An electrical test pattern has been implemented to control and measure the yield and uniformity of gate length and alignment as shown in Fig. 3. A histogram of 0.5-μm gate length and alignment accuracy control data is illustrated in

TABLE IV
EFFECTS OF OVERLAY CAPACITOR YIELD ON LNA AMPLIFIER YIELD

YIELD OF SINGLE 10 pF	YIELD OF FIVE CAPACITORS	AMPLIFIER YIELD
70%	17%	6%
80%	33%	12%
90%	59%	21%
96%	82%	29%

Total yield excluding overlay capacitors = 35 percent.

Fig. 4. An average gate length of 0.506 μm and a standard deviation of 0.04 μm have been measured from six 2-in wafers. After the gate metallization, a 2000-Å PECVD Si_3N_4 passivation layer is deposited on the active area to protect the FET and enhance its reliability.

The fabrication of MOM overlay capacitors is another key yield-limiting area for MMIC circuits. There are five 10-pF MOM capacitors in the low-noise amplifier. A small change in capacitor yield drastically changes the amplifier yield, as indicated in Table IV. For example, if the total yield excluding overlay capacitors is 35 percent, the overall amplifier yield may be dropped to 12 percent if the yield of a single capacitor is only 80 percent. A typical MOM capacitor yield of 96 percent has been obtained using a 2000-Å sputtered SiO_2 film as dielectric. The other key processes, such as airbridges and via holes, typically provide high yields (> 90 percent).

V. PERFORMANCE AND YIELD RESULTS

By using ion implantation and capless anneal techniques, good activation of the Si implant and abruptness of the doping profile were achieved. The peak concentration was about $2.6–2.9\times10^{17}$ cm^{-3} with a penetration depth of 0.18 μm. The final dc tests show excellent FET I_{DSS} uniformity for ion-implanted channels. Table V shows some of the FET uniformity and yield information on nine recent wafers fabricated by the direct ion implantation process. The standard deviation of I_{DSS} is about 11 percent, demonstrating good channel thickness control, whereas the corresponding VPE uniformity is often greater than 20 percent. An extrinsic FET transconductance of 165 mS/mm has been achieved. In Table VI, both LNA yield statistics and projected yield with process improvement are presented. More than 80 2-in wafers have been processed with a best dc yield of 35 percent. With proper dc specification control, we can usually achieve over 80 percent RF yield of dc good chips. By increasing the data base and improving this dc–RF correlation, a basis for projecting amplifier RF functional yield on the basis of on-wafer dc yield can be developed.

Performance of 35 low-noise amplifier chips randomly selected from ten wafers is illustrated in Fig. 5. These ten wafers were fabricated using the final version of the circuit design. The noise figure is measured without tuning and with a bias condition of $V_D = 3.0$ V and $I_D = 24$ mA. The

TABLE V
FET UNIFORMITY AND YIELD IN LOW-NOISE MONOLITHIC AMPLIFIERS

Lot No.	I_{DSS} of 600 m FETs			DC Yield (percent)
	Average (mA)	Standard Deviation (mA)	Uniformity (percent)	
LNA-MH-584	96.3	10.0	10.4	35
LNA-MH-585	73.1	6.7	9.1	36
LNA-MH-586	107.5	9.2	8.5	41
LNA-MH-624	95.5	13.4	14.0	35
LNA-MH-625	61.1	7.1	11.8	43
LNA-MH-626	76.7	8.5	11.0	47
LNA-MH-672	75.6	9.1	12.0	47
LNA-MH-673	72.3	11.9	16.5	54
LNA-MH-674	68.2	7.2	10.6	49
Average	80.7	9.2	11.4	43

TABLE VI
LOW-NOISE AMPLIFIER YIELD STATISTICS

PROCESS/CONTROL	YIELD	
	ACHIEVED	PROJECTED
FETs (Wg = 600 μm)	55%	70%
OVERLAY CAPACITORS (FIVE 10 pFs)	80%	85%
AIRBRIDGES	95%	95%
VIA HOLES	90%	95%
DC SPECIFICATION	75%	80%
EDGE EFFECT, DICING, AND HANDLING	75%	90%
AMPLIFIER YIELD - OVERALL	18%	35%
BEST 6-WAFER LOT	28%	
BEST SINGLE WAFER	35%	

Total processed wafers > 80. Total working amplifier chips > 3000.

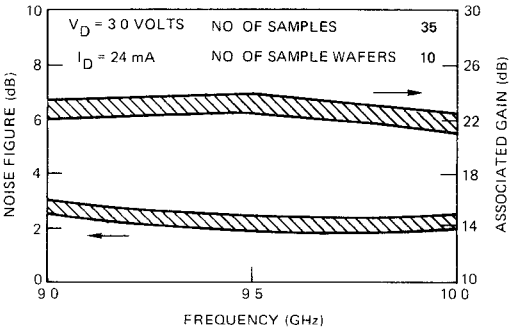

Fig. 5. Frequency response of low-noise amplifiers from ten recent wafers with the final version design.

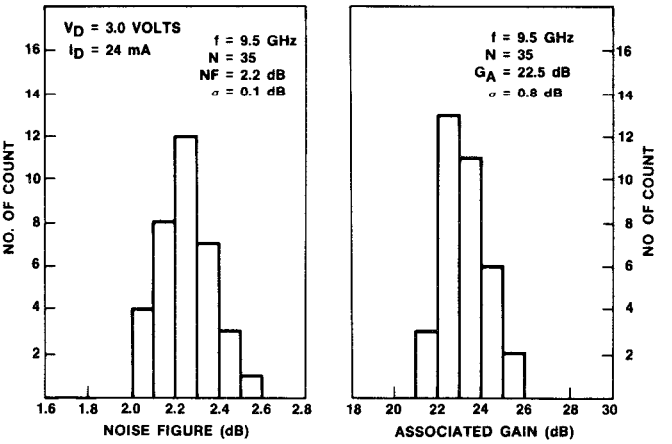

Fig. 6. Histogram of noise figure and associated gain at 9.5 GHz.

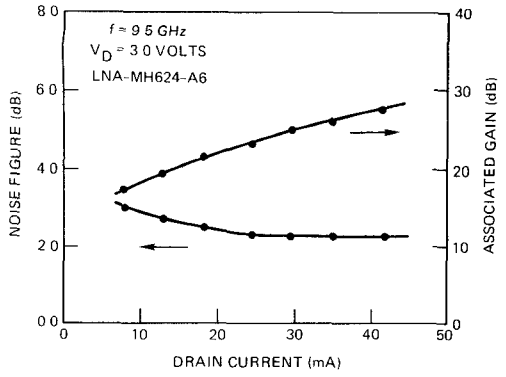

Fig. 7. Noise figure and associated gain as functions of drain current.

noise figure is less than 3.0 dB, and the associated gain is more than 20 dB across the frequency band from 9 to 10 GHz. A best noise figure of 2.0 dB with an associated gain of 24 dB has been measured at 9.5 GHz. Histograms showing the mean values and standard deviations of noise figure and associated gain at 9.5 GHz are plotted in Fig. 6. An average noise figure of 2.2 dB and a standard deviation of 0.1 dB with an associated gain of 22.5 dB and standard deviation of 0.8 dB have been obtained from 35 samples. The noise figure and associated gain as a function of drain current are shown in Fig. 7. It indicates that higher gain with the same noise figure can be achieved at higher drain current between 24 mA and 42 mA.

VI. Cost Reduction Trend

The cost of GaAs monolithic IC chips will decrease as the technology matures and manufacturing throughput increases. Since the implanted LEC wafer has been adopted as the baseline material approach, we have gained the benefits of both yield and cost when compared to VPE materials. Our recent data show that implanted wafers have at least a 10 percent higher device yield than VPE wafers because of better uniformity. Combining this yield factor and the lower cost of implanted materials. we can reduce the chip cost by a factor of two on *X*-band amplifiers. Process control monitoring and sensitivity analysis allow us to further improve yield by better controlling the process and designing a more tolerant circuit. In addition, ordinary silicon process techniques, such as cassette handling, microprocessor control, and automated equipment, must be implemented in GaAs processing. On this basis, we believe that an overall yield higher than 30 percent and a throughput greater than 100 wafers per week are realistic.

Fig. 8 shows the estimated MMIC chip cost in the future manufacturing environment with at least 100 wafer starts per week. At present, the chip cost is typically above $100, with an average yield of 15 percent for 2-in VPE wafer process. Fig. 8 also illustrates the chip cost as a function of yield for six different cases. It indicates that a low cost can be achieved with the same yield level using 3-in ion-implanted materials, which is our proposed baseline approach. As long as the yield is maintained above 20 percent with the size of a lot larger than five 3-in wafers,

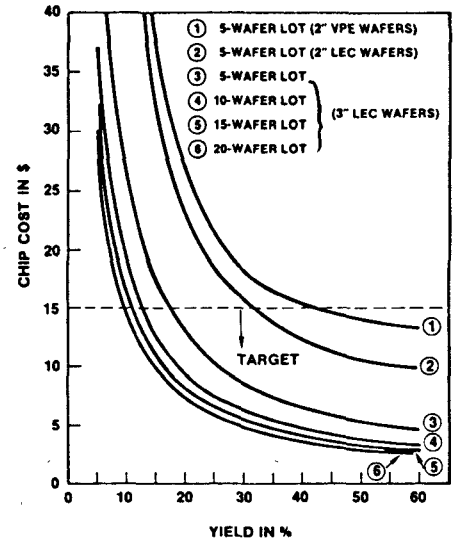

Fig. 8. Estimated MMIC chip cost in the future manufacturing environment.

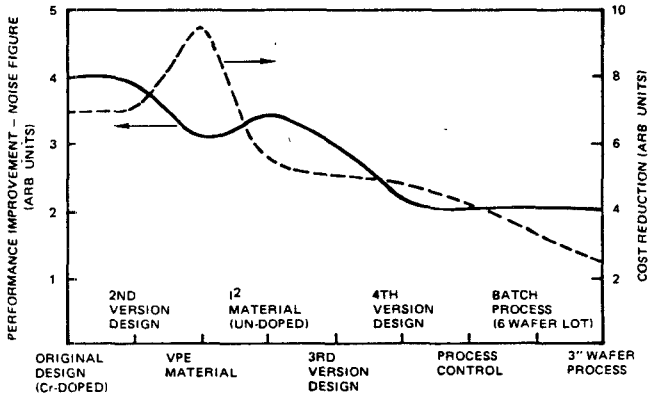

Fig. 9. Trends of LNA performance improvement and cost reduction during the technology development stage.

the cost of the chips will be below $15 targeted in the near future.

One recent example of cost reduction is the *X*-band low-noise amplifier (LNA). We have recently implemented process control and a 3-in wafer batch process and fabricated LNA with the final version of circuit design. The trends of cost reduction and performance improvement shown in Fig. 9 indicate that the cost of LNA chips was reduced by a factor of three during the development stage. At the same time, the LNA circuit noise figure performance was also improved by a factor of two. The yield and performance improvements are mainly caused by the process control and modification and the better matching circuit design.

VII. Conclusions

A high-performance *X*-band monolithic low-noise amplifier with low cost ion-implanted MESFET technology has been demonstrated. Through improvements in material/process uniformity, process control monitoring, and wafer handling, we can further enhance the overall yield without degrading the projected high performance of the amplifier circuit. An extrinsic FET transconductance

of 165 mS/mm and a best dc yield of 35 percent have been achieved. A typical noise figure of 2.0 to 2.4 dB with associated gain of 20 to 23 dB has been measured at 9.5 GHz.

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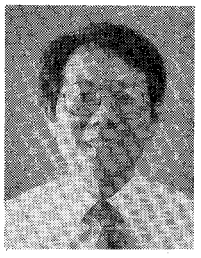

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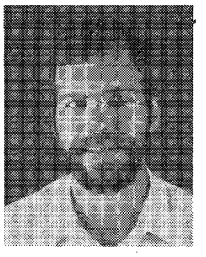

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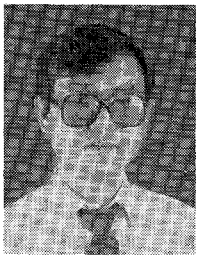

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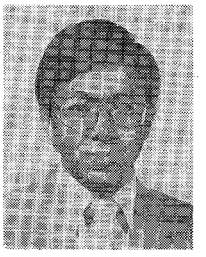

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